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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,345	03/02/2000	Sidney Larry Anderson	15114-052310	4253

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EXAMINER

PAREKH, NITIN

ART UNIT PAPER NUMBER

2811

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.		Applicant(s)	
	09/517,345		ANDERSON ET AL.	
	Examiner		Art Unit	
	Nitin Parekh		2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 February 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 71-90 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 71-90 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 71-73, 76-84, 86, 87, 89 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Lau (see "Chip on Board Technologies for Multichip Modules" edited by John H. Lau, published by Chapman & Hall, 1994) and Futakuchi (US Pat. 6308938).

Regarding claims 71-73, 78 and 79, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3A) having a first thickness
- a metallized polymer layer/flexible dielectric tape/substrate (59/60 in Fig. 3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3A) disposed between the silicon die and the first side of the substrate/metallized polymer layer where the transition medium/support structure has a second thickness
- the die being coupled to the transition medium through an adhesive (64 in Fig. 3A; Col. 9, line 65)

- a plastic encapsulant/mold cap encapsulating the transition medium and the die (mold cap not numerically referenced in Fig. 3A; see 86 in Col. 8, line 40), and
- the BGA package being capable to be coupled to a printed circuit board (PCB) (Fig. 3A; Col. 7, line 15- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller further teaches using a single transition medium/support structure comprising:

- a second thickness/layer of 100-250 microns (Col. 9, line 49) or using a plurality of those layers (Col. 11, line 12), and
- the transition medium/support structure comprising a variety of material including conventional FR-4/epoxy resin (Col. 10, lines 18-28).

Schueller fails to teach the mold cap and the transition medium expand and contract at approximately the same rate in response to temperature changes so as to reduce thermal stress on the silicon die during thermal cycling.

Lau teaches conventional materials including a FR4/epoxy resin having a CTE ranging from $5-19 \times 10^{-6}/^{\circ}\text{C}$ or a PCB CTE as high as $20 \times 10^{-6}/^{\circ}\text{C}$, a silicon chip/die having that around $3.0 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 52, Table 1-7), a mold cap/molding compound having that around $17 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 507) and an adhesive/silicone material having that from $50-150 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 507, Table 12-2).

Futakuchi teaches a conventional glass-reinforced epoxy resin material having CTE of about $16 \times 10^{-6}/^{\circ}\text{C}$ (Col. 6, line 14).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the mold cap and the transition medium having the CTE in

the same range of $7-15 \times 10^{-6}/^{\circ}\text{C}$ or about equal value around $16-17 \times 10^{-6}/^{\circ}\text{C}$ or less than that of the PCB and greater than that of the silicon die, such thermal property value/range providing approximately the same thermal expansion/contraction rate to provide functions of reduced thermal/mechanical stress, reduced defects and improved reliability during thermal cycling and temperature variations in subsequent processing as taught by Lau and Futakuchi so the thermal/electrical performance and reliability can be improved in Schueller's IC package.

Regarding claim 76, Schueller, Lau and Futakuchi teach substantially the entire claimed structure as applied to claim 71 above, wherein Schueller further teaches the die being disposed approximately near the middle of a package having a thickness where the package thickness is defined by the thickness of the substrate/metallized polymer layer/tape and that of the plastic encapsulant/mold cap (Col. 8, line 40; Fig. 3A), but fail

to explicitly teach the die being disposed approximately equally spaced from the bottom of the metallized polymer layer and the top of the plastic encapsulant.

The determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the encapsulant such that die is disposed approximately equally spaced from the bottom of the metallized polymer layer and the top of the plastic encapsulant so that the desired thermal/mechanical stress can be reduced and the and the reliability of the package can be improved in Futakuchi, Lau and Schueller's IC package.

Regarding claim 77, the movement/position of the die during thermal cycling do not distinguish over Schueller, Futakuchi and Lau, because only the final product/structure is relevant, not the movement of the die during "thermal cycling", "high temperature curing", "soldering/bonding on the PWB or subsequent processing", etc. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186

USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 80-82, Schueller, Futakuchi and Lau teach substantially the entire claimed structure as applied to claim 71, above, wherein Schueller further teaches the

metallized polymer layer/flexible dielectric tape having conventional dielectric and conductive layers (60 and 59 respectively in Fig. 3A; Col. 7) and solder balls being mounted to the second side of the metallized polymer layer and electrically contacting the etched circuit in a conductive layer of the tape carrier (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claims 83, 86 and 87, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3A) having a first thickness
- a metallized polymer layer/flexible dielectric tape/substrate (59/60 in Fig. 3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3A) disposed between the silicon die and the first side of the substrate/metallized polymer layer where the transition medium/support structure has a second thickness
- the die being coupled to the transition medium through an adhesive (64 in Fig. 3A; Col. 9, line 65)
- a plastic encapsulant/mold cap encapsulating the transition medium and the die (mold cap not numerically referenced in Fig. 3A; see 86 in Col. 8, line 40), and
- the BGA package being capable to be coupled to a printed circuit board (PCB) (Fig. 3A; Col. 7, line 15- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller further teaches using a single transition medium/support structure comprising:

- a second thickness/layer of 100-250 microns (Col. 9, line 49) or using a plurality of those layers (Col. 11, line 12), and
- the transition medium/support structure comprising a variety of material including conventional FR-4/epoxy resin (Col. 10, lines 18-28).

Schueller fails to teach the mold cap and the transition medium expand and contract at approximately the same rate in response to temperature changes.

Lau teaches conventional materials including a FR4/epoxy resin having a CTE ranging from $5-19 \times 10^{-6}/^{\circ}\text{C}$ or a PCB CTE as high as $20 \times 10^{-6}/^{\circ}\text{C}$, a silicon chip/die having that around $3.0 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 52, Table 1-7), a mold cap/molding compound having that around $17 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 507) and an adhesive/silicone material having that from $50-150 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 507, Table 12-2).

Futakuchi teaches a conventional glass-reinforced epoxy resin material having CTE of about $16 \times 10^{-6}/^{\circ}\text{C}$ (Col. 6, line 14).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the mold cap and the transition medium having the CTE in the same range of $7-15 \times 10^{-6}/^{\circ}\text{C}$ or about equal value around $16-17 \times 10^{-6}/^{\circ}\text{C}$ or less than that of the PCB and greater than that of the silicon die, such thermal property value/range providing approximately the same thermal expansion/contraction rate to provide functions of reduced thermal/mechanical stress, reduced defects and improved reliability in response to temperature changes as taught by Lau and Futakuchi so the

thermal/electrical performance and reliability can be improved in Schueller's IC package.

Furthermore, regarding claim 83, the movement/position of the die during thermal cycling do not distinguish over Schueller, Futakuchi and Lau, because only the final product/structure is relevant, not the movement of the die during "thermal cycling", "high temperature curing", "soldering/bonding on the PWB or subsequent processing", etc. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marrosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 84, Schueller, Futakuchi and Lau teach substantially the entire claimed structure as applied to claim 83 above, wherein Schueller further teaches the die being disposed approximately near the middle of a package having a thickness where the package thickness is defined by a third thickness of the plastic encapsulant/mold cap and a forth thickness of the metallized polymer layer/tape (Col. 8, line 40; Fig. 3A), such configuration providing reduced deformation/warping due to temperature variations/thermal cycling.

Furthermore, the determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to have the die being disposed near middle of the package so that the thermal/mechanical stress can be reduced and the and the reliability of the package can be improved in Lau, Futakuchi and Schueller's IC package.

Regarding claims 89 and 90, Schueller, Futakuchi and Lau teach substantially the entire claimed structure as applied to claim 83, above, wherein Schueller further teaches the metallized polymer layer/flexible dielectric tape having conventional dielectric and conductive layers (60 and 59 respectively in Fig. 3A; Col. 7) and solder balls being mounted to the second side of the metallized polymer layer and electrically contacting the etched circuit in a conductive layer of the tape carrier (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

3. Claims 74 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Lau (see "Chip on Board Technologies for Multichip Modules" edited by John H. Lau, published by Chapman & Hall, 1994) and Futakuchi (US Pat. 6308938) as applied to claims 71 and 83 above, and further in view of Zenner et al. (US Pat. 6246010).

Regarding claim 74, Schueller, Lau and Futakuchi teach substantially the entire claimed structure as applied to claims 71 and 83 above, except the first thickness of the silicon die being less than a second thickness of the transition medium.

Zenner et al. teach using a high density/thin package having a die thickness/first thickness where the die has been thinned/lapped to about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55; Col. 2-4) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first thickness of the silicon die being less than a second thickness of the transition medium as taught by Zenner et al. so that the thermal stress can be reduced and the functionality/reliability can be improved in Futakuchi, Lau and Schueller's IC package.

Regarding claim 85, Schueller, Lau, Futakuchi and Zenner et al. teach substantially the entire claimed structure as applied to claims 74 and 83 above.

4. Claims 75 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949), au (see "Chip on Board Technologies for Multichip Modules" edited by John H. Lau, published by Chapman & Hall, 1994) and Futakuchi (US Pat. 6308938) as applied to claims 71 and 83 above, and further in view of Freyman et al. (US Pat. 5985695).

Regarding claim 75, Schueller, Lau and Futakuchi teach substantially the entire claimed structure as applied to claim 71 above, except a first and a second edge of the transition medium is coincident with those of the die.

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and second edge of the transition medium being coincident with those of the silicon die respectively so that the thermal stress can be reduced, the functionality/reliability of the package can be improved and processing can be simplified in Futakuchi, Lau and Schueller's IC package.

Regarding claim 85, Schueller, Lau, Futakuchi and Freyman et al. teach substantially the entire claimed structure as applied to claims 75 and 83 above.

Response to Arguments

5. Applicant's arguments filed on 2-7-07 have been fully considered but they are not persuasive.

A. Applicant contends that Futakuchi does not disclose any specific value of the CTE of the sealing resin layer 5 and suggests using glass fiber-reinforced epoxy having a CTE of 16×10^{-6} for the sealing resin layer 5.

However, as explained in the rejections above, Schueller teaches using the transition medium/support structure comprising a variety of material including conventional FR-4/epoxy resin (Col. 10, lines 18-28).

Futakuchi teaches the reinforcement medium/base made of the conventional epoxy resin material, such conventional glass-reinforced epoxy resin material having CTE of about $16 \times 10^{-6}/^{\circ}\text{C}$ (see Col. 6, line 14) and (b) Lau teaches the conventional mold cap/molding compound having a CTE around $17 \times 10^{-6}/^{\circ}\text{C}$ (see pp. 507).

Therefore, the combination of Schueller, Lau and Futakuchi teach the epoxy resin based material having a CTE around $16-17 \times 10^{-6}/^{\circ}\text{C}$ being used as the transition material and the mold cap such that the transition medium expand and contract at approximately the same rate in response to temperature changes to reduce the thermal stress for the IC package.

B Applicant contends that at none of the cited references disclose or suggest an integrated circuit package in which the thickness of the silicon die is less than the thickness of the transition medium.

However, as explained in the rejections above, Schueller teaches the transition medium/support structure having the second thickness/layer of 100-250 microns (Col. 9, line 49). Zenner et al. teach the die thickness being less than 100 microns or 20 microns (see Col. 2, line 15-22; Col. 3, line 55).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rich Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

4-6-07



NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800